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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,254	06/14/2001	Fwu-Jiun Hshieh	GS 134	6677

27774 7590 02/13/2003

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[REDACTED] EXAMINER

MONDT, JOHANNES P

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2826

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.	09/881,254	
Examiner	HSHIEH ET AL	
Johannes P Mondt		Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 22 November 2002.  
2a) This action is FINAL.      2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-16, 25 and 26 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) Claim(s) \_\_\_\_\_ is/are allowed.  
6) Claim(s) 1-16 and 25-26 is/are rejected.  
7) Claim(s) \_\_\_\_\_ is/are objected to.  
8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
    If approved, corrected drawings are required in reply to this Office action.  
12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
    1. Certified copies of the priority documents have been received.  
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.  
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
    a)  The translation of the foreign language provisional application has been received.  
15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)      4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)      5) Notice of Informal Patent Application (PTO-152)  
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.      6) Other: \_\_\_\_\_

**DETAILED ACTION*****Response to Amendment***

Amendment A filed 11/22/2002 and entered as Paper No. 8 forms the basis of this office action. In view of the cancellation or deletion of claims 17-24 in Amendment A and the addition of new claims 25-26, claims 1-16 and 25-26 are currently pending in the application. For comments on Remarks by Applicant see "Response to Arguments" included below.

***Response to Arguments***

1. Applicant's arguments filed 11/22/2002 have been fully considered but they are not persuasive. In particular, Vinson states that electrical symmetry is retained by the absence of a graded dopant concentration in the channel. Aforementioned retainment is simply not possible without substantially the same dopant concentrations in the source and drain regions abutting the channel to a depth of a Debye screening length (see for instance any text book discussing Fermi or electron gas physics including those in the solid-state device area, such as Sze ("Physics of Semiconductor Devices", second edition, pp. 74-81)), because the space charge fields exerted by the source and drain region's dopants in the abutting channel regions otherwise would inherently cause electrical asymmetry to a depth over a Debye length within the channel region. The alleged failure of Vinson to teach said symmetry of said doping profile to extend to at least a portion of the source and drain regions is thus completely implied by the text in Vinson as cited by the examiner, i.e., column 6, lines 28-32. Applicant also alleges that Vinson uses two fundamentally different techniques to form the source and drain

regions. However, aspects of method of making are irrelevant, because only the final structure is patentable through the present device invention as elected in Paper No. 4. Furthermore, instead of specifically taking issue with the stated motivation ("for the specific purpose of retaining electrical symmetry" with specific reference to Vinson), Applicant merely alleges the absence of motivation. This traverse is therefore unacceptable. All traverses by Applicant rely on abovementioned points.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. ***Claims 1 – 4, 6 – 8, and 10 – 16 are rejected*** under 35 U.S.C. 103(a) as being unpatentable over Mogi et al (4,250,519) in view of Vinson (4,116,720).

*With regard to claims 1 – 3:* With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:

a drain region 24 (cf. column 3, lines 3-5) of first conductivity type (n type);  
a body region 26 of second conductivity type (p type) provided over said drain region, said drain region and said body region forming a first junction;  
a source region 27 (cf. column 3, lines 13-14) of first conductivity type provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region 27, through said body region 26 and into said drain region 24 (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising an insulating layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a conductive region 32 (cf. column 3, line 20) within said trench adjacent said insulating layer, and in which gate region gate metal, particularly aluminum metal (cf. column 3, line 21) is allowed to be adjacent said conductive region (the additional limitation as defined by *claim 3* is thus anticipated by Mogi et al).

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3) (the additional limitation as defined by *claim 2* is thus anticipated by Mogi et al).

*Mogi et al do not necessarily teach* the further limitation defined ad (b) in claim 1 of Applicants. *However, in a patent on a vertical MOSFET with groove alias trench (cf. title and abstract) and for the specific purpose of retaining electrical symmetry (cf. column 6, line 32), Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer without additional doping (cf. column 3, lines 5-6 and line 24) with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body*

region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include aspect ad (b) as taught by Vinson.

*With regard to claim 4:* body region 26 in Mogi et al is a lightly P-doped semiconductor (epitaxial) layer (cf. column 3, lines 5-6), any doped semiconductor region has dopants, while each dopant is a generation-recombination center. Thus the further limitation of claim 4 does not distinguish from the prior art as taught by Mogi et al.

*With regard to claim 6:* source, drain, and body regions as taught by Mogi et al are doped silicon regions (cf. column 2, line 61 – 63, column 3, lines 13 – 14 and 24). Therefore, the further limitation as defined by claim 6 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 7:* said conductive region 32 as taught by Mogi et al can be made of polysilicon (cf. column 3, lines 20-23). Therefore, the further limitation as defined by claim 7 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 8:* said insulating layer 29 as taught by Mogi et al is a silicon dioxide layer (cf. column 3, lines 22-23). Therefore, the further limitation as defined by claim 8 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 10:* the examiner takes official notice that in general, a gate insulator layer of silicon dioxide formed using CVD or PVD has many dangling bonds within the film. These become interface states or fixed charges within the insulating layer. Applicants' further limitation as defined by claim 10 is therefore a result of standard fabrication procedures of said insulating layer and does not distinguish over the prior art.

*With regard to claim 11:* said source and drain regions as taught by Mogi et al are heavily doped regions (cf. column 3, lines 3-4 and 13), while said body region 26 (cf. column 3, lines 5-6) as taught by Mogi et al is a lightly doped region. It follows that said source and drain regions have peak net doping concentrations that are greater than a peak net doping concentration of said body region. Therefore, the further limitation as defined by claim 11 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 12:* said first conductivity type taught by Mogi et al is n type and said second conductivity type as taught by Mogi et al is p type, as

detailed above in the discussion of claim 1. Therefore, the further limitation as defined by claim 12 does not distinguish over the prior art as taught by Mogi et al.

*With regard to claim 13: Mogi et al do not necessarily teach the further limitation of claim 13. However, it has long been known that source and drain can be made in the present art by a single irradiation by dopants, as actually taught by Vinson, who teaches the use of an ion beam for the purpose of exploiting ion implantation to simultaneously, hence in a cost-effective manner, create the heavily doped source and drain regions by use of the same dopant material (see Fig. 2D, and column 3, lines 42-50). Motivation to combine the invention by Mogi et al with the teaching, in this regard, by Vinson stems at least from the aforementioned cost-effectiveness. Because the devices of Mogi et al and Vinson are both V-MOS transistors the geometric similarities are conducive to the implementation of Vinson's teaching, hence success in the aforementioned implementation can be reasonably expected.*

*With regard to claim 14: With reference to Fig. 3: Mogi et al teach a trench MOSFET transistor device comprising:*  
a silicon drain region 24 (column 3, lines 13-14) of N-type conductivity;  
a silicon body region 26 of P-type conductivity (cf. column 3, lines 5-6)  
provided over said drain region, said drain region and said body region forming a first junction;

a silicon source region 27 (cf. column 3, lines 3-4) of N-type conductivity provided over said body region, said source region and said body region forming a second junction;

source metal 34 (cf. column 3, line 24) disposed on an upper surface of said source region;

a trench (V-groove; cf. column 3, line 9) extending through said source region, through said body region and into said drain region (cf. Figs. 1 and 3); and

a gate region 29/32 (cf. column 3, lines 20-23) comprising a silicon dioxide layer 29 (cf. column 3, line 23) lining at least a portion of said trench and a doped polycrystalline silicon region 32 (cf. column 3, line 20) within said trench adjacent said silicon dioxide layer,

wherein said body region is separated from said source metal (i.e., 26 and 34 do not share a common border line; see Fig. 3) by said source region 27 (cf. Fig. 3). In the invention taught by Mogi et al the source and drain region have peak doping densities high (cf. column 3, lines 13-14) compared with the doping density of the (epitaxial) body region 26 (cf. column 3, line 46).

*Mogi et al do not necessarily teach the further limitations defined by ad (b) and (d).*

*However, with regard further limitation (b) it has long been shown that a most efficient method of making source and drain in vertical trench MOSFET devices comprises the use of a single ion beam irradiating the semiconductor*

material to dope source and drain simultaneously and with the same dopant as defined by the beam ions as shown by Vinson in a patent on a vertical MOSFET with groove alias trench (cf. title and abstract); while

*with regard to further limitation (d), for the specific purpose of retaining electrical symmetry (cf. column 6, line 32),* Vinson teaches the body region 21 (cf. Fig. 2E) to be a lightly P-doped silicon epitaxial layer without additional doping (cf. column 3, lines 5-6 and line 24) and with a doping profile along a line normal to upper and lower surfaces of said device such that, within said body region and within at least a portion of said source and drain regions, the doping profile (characterized by constant doping concentration) on one side of a center plane of the body region is symmetric with the doping profile on an opposite side of the center plane (cf. column 6, lines 28-32). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include aspects ad (b) and (d) as taught by Vinson. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Mogi et al so as to include the further limitations ad (b) and (d); hence claim 14 is unpatentable over Mogi et al in view of Vinson.

*With regard to claims 15-16:* Mogi et al use arsenic as the said doping material, while the examiner takes official notice that phosphor is also standardly used for the same purpose, while having the advantage of being less toxic.

*With regard to claim 26:* Mogi et al do teach the trench MOSFET transistor device to comprise a plurality of source regions which are shorted to one

another, specifically the source regions 23 contacting the respective bottom portions of the trenches of trench MOS transistor devices 38 and 39.

3. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mogi et al and Vinson as applied to claim 4 above, and further in view of Seki (5,025,293). As detailed above, claim 4, on which claim 5 depends, is unpatentable over Mogi et al in view of Vinson, neither of whom, however, necessarily teach the further limitation as defined by claim 5. *However, the use of gold, or as a non-exclusive alternative platinum, as a dopant in semiconductor material as a material to provide generation-recombination centers for the purpose of shortening charge carrier lifetime and thereby reducing turn-off time* has long been known in the art of semiconductor device technology, as witnessed by Seki who teach the application of either gold or platinum to facilitate recombination of electrons and holes of this purpose in a vertical MOSFET. Although the device taught by Seki et al is not a trench type vertical MOSFET the same desirability of short turn-off time qualifies as a legitimate advantage and hence said purpose is valid for Applicants' invention as well. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 4 at the time it was made so as to include the further limitation of claim 5.

4. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mogi et al and Vinson as applied to claim 6 above, and further in view of Wolf et al (ISBN 0-

9616721-6-1). As detailed above, claim 6 (on which claim 9 depends) is unpatentable over Mogi et al in view of Vinson.

*Neither Mogi et al nor Vinson necessarily teach the further limitation as defined by claim 9.*

*However, as explained in standard textbooks such as Wolf et al, the use of silicon oxynitride as semiconductor insulation layer has long been recognized to have the following advantages: the properties of silicon oxynitrides can be tailored, through the stoichiometric variables pertaining to the oxygen and nitrogen contents, to improve (a) thermal stability, (b) lower film stress, and (c) crack resistance.*

*All of the above three advantages have relevance for the gate insulating layer in the invention by Applicants. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 6 so as to include the further limitation as defined by claim 9.*

5. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mogi et al (4,250,519) and Vinson (4,116,720) as applied to claim 1 above, and further in view of Baliga (ISBN: 0-89464-799-7) and van Loon et al (4,219,835). As detailed above, claim 1 (on which claim 25 depends) is unpatentable over Mogi et al in view of Vinson. Neither Mogi et al nor Vinson necessarily teach the further limitation as defined by claim 25. However, it has long been known in the art to use source-body contact for the specific purpose to reduce second breakdown through a reduction in the voltage across the emitter-base junction of the parasitic bipolar transistor in MOSFET devices, as

discussed in Baliga (page 318, second paragraph). Van Loon et al actually implement said source-body contact for the particular case of VMOSFET devices (cf. abstract, fourth sentence, column 2, lines 41-44 and column 3, lines 24-29).

*Motivation* to include the teaching by Baliga and van Loon et al in this regard into the invention as essentially taught by Mogi et al is the advantage to increase the breakdown voltage, which is commonly understood to be a generic advantage for all MOSFET devices. *Combination* of the aforementioned teachings with the aforementioned invention is straightforward through the implementation of a metal connection between source and body. Success in implementing said combination can therefore be reasonably expected.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: S.M. Sze, "Physics of Semiconductor Devices", Second Edition, John Wiley & Sons, New York (1981)); pp. 74-81.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM  
February 3, 2003

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